3D Simulation and Analysis of the Radiation Tolerance of Voltage Scaled Digital Circuit

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Abstract*— In recent times, dynamic supply voltage scaling (DVS) has been extensively employed to minimize the power and energy of VLSI systems. Also, sub-threshold circuits are becoming more popular. At the same time, the reliability of VLSI systems has become a major concern under Single Event Upsets (SEUs). SEUs are very problematic even for circuits operating at nominal voltages. With the increasing demand for low power reliable systems, it is therefore necessary to harden DVS and sub-threshold circuits efficiently. In this paper, we perform 3D simulations of radiation particle strikes in an inverter implemented using DVS and sub-threshold design. We analyze the sensitivity of the inverter to radiation particle strikes by varying the inverter size, the inverter load, the supply voltage (VDD) and the energy of the radiation particles. From these 3D simulations, we make several observations which are important to consider during radiation hardening of DVS and sub-threshold circuits. Based on these observations, we propose several guidelines for radiation hardening of DVS and sub-threshold circuit designs. These guidelines suggest that the traditional radiation hardening approaches need to be revisited for DVS and sub-threshold designs. We also propose a charge collection model for DVS circuits. Our model can accurately estimate (with an average error of 6.3%) the charge collected at the output of a gate for different supply voltages and different gate sizes for medium and high energy particle strikes. The parameters of our charge collection model can be included in SPICE model cards of transistors, to improve the accuracy of SPICE based radiation simulations for DVS circuits.

I. Introduction

Single event upsets (SEUs) have become increasingly problematic for both combinational and sequential VLSI circuits in the deep sub-micron (DSM) era [1], [2], [3], [4]. This is due to continuously decreasing feature sizes, lower supply voltages and higher operating frequencies, which cause a reduction in the noise margins of VLSI designs. At the same time, power has become a major issue in computing [5]. Low energy solutions are desired for many applications such as Systems-on-chip (SoC), microprocessors, wireless communication circuits, etc. Both the dynamic and the leakage components of the power consumption of a CMOS circuit depend upon the supply voltage; both decrease at least quadratically with decreasing supply voltages. Therefore, in recent times, it is common to decrease the supply voltage value in the non-critical parts of VLSI systems, in order to reduce the power and energy consumption.

Modern VLSI systems extensively employ dynamic voltage scaling (DVS) to meet the variable speed/power requirements at different times during their operation [6], [7], [8]. DVS helps in reducing the circuit power consumption especially when high speed circuit operation is not desired. Today, VLSI circuits are also operated in the sub-threshold region of operation for a widening class of applications which demand extreme low power consumption and can tolerate larger circuit delays [9], [10], [11]. Sub-threshold circuits operate with a supply voltage less than or equal to the device threshold voltages. Since both DVS and sub-threshold circuits are extensively used to reduce power consumption, their susceptibility to radiation particle strikes can significantly impact the reliability of such VLSI systems. Hence, it is important to analyze the effects of radiation particle strikes on DVS and sub-threshold circuits. Based on the result of such an analysis, these circuits can be hardened against radiation strikes to improve their reliability.

DVS and sub-threshold circuits have not received much attention in terms of their susceptibility to radiation particle strikes. The authors of [12] used a 3D device simulation tool to study the radiation induced transients and estimate the soft error rate (SER) in static random access memory (SRAM) cells. In [13], an experimental study of the effects of heavy ions in highly scaled commercial SOI PowerPC microprocessors was conducted. Microprocessors implemented using different technology nodes as well as different core voltage were used in the experiment. It was also observed in [13] that the reduction of feature size from $0.18\mu m$ to $0.13\mu m$ and core voltage from 1.6V to 1.3V had little effect on the soft error rate. The sensitivity of various commercial SRAM devices to radiation, as a function of their supply voltages was analyzed in [14]. An increase in the radiation susceptibility of SRAMs with decreasing supply voltage was observed. The SRAMs used in these experiments were fabricated in older technologies i.e. the feature sizes were greater than $0.18\mu m$. The authors of [15] analyzed the dependence of soft error rate on the critical charge[1] and supply voltage for a $0.6\mu m$ CMOS process. In both [14] and [15], the analysis was performed through experiments and simulations for supply voltage values much higher than the threshold voltage (the minimum supply voltage values used was 1.5V in [14] and 2.2V in [15]). Hence, the results of [14], [15] cannot be used directly to predict the susceptibility of devices at lower (and sub-threshold) voltages. Also, older process technologies were analyzed in [14], [15] and it is expected that recent deep submicron

[1]The minimum amount of charge that is required to cause an SEU event is referred to as critical charge.

technologies can exhibit very different behavior to radiation particle strikes than preceding processes [4]. In [13], [14], [15], no circuit level radiation hardening guidelines were proposed. In contrast, we model and analyze radiation strikes in current technologies, providing hardening guidelines based on our findings.

In this paper, we have analyzed radiation particle strikes in DVS and sub-threshold circuits. We performed 3D simulations for radiation particle strikes in an inverter, using Sentaurus-DEVICE [16]. Sentaurus-DEVICE is a mixed-level device and circuit simulator. Our simulations modeled the NMOS transistor of the inverter in the 3D device domain (to simulate a radiation particle in the NMOS transistor) and the PMOS transistor was modeled using a SPICE-like compact model in the circuit domain. We varied the inverter size, the inverter load, the supply voltage (VDD) and the energy of the radiation particle. From these 3D simulations, we make several observations which are important to consider during radiation hardening of DVS and sub-threshold circuits. The results suggest that the conventional approach adopted by several circuit hardening techniques [17], [18], [19], [20] (i.e to use the same radiation induced current or same amount of charge collection across different circuit scenarios such as node capacitance, supply voltages, etc) may lead to a pessimistic hardened design. From the observations we made through 3D simulations, we propose several guidelines for radiation hardening of DVS and sub-threshold circuit design. From these 3D simulations, we also propose a charge collection model for DVS circuits to improve the accuracy of simulation of a radiation particle strike in SPICE.

The main contributions of this paper are:

- Through 3D simulations of a radiation particle strike at the output of an inverter, we made several observations (described in Section IV), some of which have not been reported to date. We also made some observations which are somewhat intuitive.
- Based on the observations made, we present several design guidelines for DVS and sub-threshold circuits (desribed in Section IV). These guidelines suggest that the traditional radiation hardening approaches cannot be directly used for hardening DVS and sub-threshold circuits.
- We present an accurate charge collection model for DVS circuits. Our model can estimate the charge collected at the output of a gate for different supply voltages (VDD $> 2 \cdot V_T$) and different gate sizes for medium and high energy particle strikes with an average error of 6.3%. The parameters of our charge collection model can be added to SPICE transistor model cards to improve the accuracy of evaluation of radiation susceptibility of DVS circuits in SPICE.

The rest of the paper is organized as follows. Section II briefly discusses about the charge deposition and collection mechanism during a radiation particle strike. In Section III we describe our 3D simulation setup to simulate a radiation particle strike at the output of inverter. In Section IV we present experimental results and discuss several observations we made. We also present corresponding design guidelines in this section. Finally, we present conclusions in Section V.

II. Background

Much research has been done over more than two decades, to understand the charge disposition and collection mechanisms due a radiation particle strike in VLSI designs [21], [22], [23], [24], [4]. Numerous experiments have been performed, and different theoretical methods have been used to study the effects of radiation particle strikes and to measure the transients induced by these strikes. Reverse-biased p-n junction regions in VLSI design are the most sensitive to radiation particle strikes. This is due to the presence of a high electric field in the reverse biased p-n junction depletion region, which can efficiently collect the radiation induced charge.

A radiation particle generates electron-hole pairs along its path as it passes through a semiconductor material. The energy transferred by the radiation particle is described by its linear energy transfer (LET) value. LET is defined as the energy transferred (for electron-hole pair generation) by the radiation particle per unit length normalized by the density of the target material (for VLSI designs, this is the density of Silicon). Thus the unit of LET is MeV-cm^2/mg. The LET of a radiation particle also corresponds to the charge deposited by the radiation particle per unit length. In silicon, a radiation particle with an LET of 97 MeV-cm^2/mg can deposit $1pC/\mu m$. Heavy ions[2] and alpha-particles primarily deposit charge in the semiconductor by direct ionization, whereas protons and neutrons typically deposit charge by indirect ionization [4], [3], [25]. After the charge is deposited by a radiation particle strike, it may get collected through different charge collection mechanisms: *drift-diffusion, bipolar effect and alpha-particle source-drain penetration effect (ALPEN)* [21], [22], [23], [24], [4]. For brevity, we are not describing these charge collection mechanisms. The readers are encouraged to refer to the papers [4], [26], [22], [23] for detailed description of these charge collection mechanisms.

The charge collected at the drain node of a transistor due to a radiation particle strike may induce voltage and current transients in the circuit in which this transistor is present. Specifically, the radiation induced current flows from the n diffusion to p diffusion. Traditionally, the radiation induced current is modeled by a double-exponential current pulse [27] for circuit level simulations. The expression for this pulse is

$$i_{seu}(t) = \frac{Q}{(\tau_\alpha - \tau_\beta)}(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}) \quad (1)$$

Here Q is the amount of charge collected as a result of the ion strike, while τ_α is the collection time constant for the junction and τ_β is the ion track establishment constant. This current pulse is injected at a node in a circuit to simulate a radiation particle strike at that node. In the deep submicron

[2]Heavy ion are ions whose atomic number is greater than or equal to 2 [4]

devices, the radiation induced current may be very different from this double exponential pulse [23], [28]. Therefore, for an accurate analysis, device-level simulations of radiation particle strikes in transistors have to performed. Mixed-level simulators are widely used to simulate a radiation particle strike. In such simulations, the device struck by the radiation particle is modeled in the "device domain" (i.e. using 3-D device simulation), while the rest of the circuit is represented by the SPICE like compact circuit models. In this paper, we use Sentaurus-DEVICE which is a Mixed-level simulator.

III. Simulation Setup

In this paper, we consider a radiation particle strike at the NMOS transistor of an inverter (INV) shown in Figure 1. INV is implemented in a 65nm bulk technology. The input of the INV is at GND and hence, the PMOS transistor is ON and the NMOS transistor is OFF. We used Sentaurus-DEVICE [16] which is a mixed-level device and circuit simulator to simulate the INV of Figure 1 with a radiation particle strike at the NMOS transistor. We modeled the NMOS transistor of the INV in the 3D device domain as described in Section III-A. The PMOS transistor of INV is modeled using a SPICE model in the circuit domain, obtained from PTM [29]. Note that we did not simulate a particle strike at the PMOS transistor since, we expect that a particle at the PMOS transistor will also give us similar results as obtained from a particle strike at the NMOS transistor.

To analyze the sensitivity of sub-threshold circuits and circuits which employ DVS to radiation particle strikes, we varied the supply voltage (VDD) of INV in our simulations. We also varied the size of INV of Figure 1 as well as the LET of the radiation particle, to simulate different radiation scenarios in a circuit. The supply voltage values we used are 0.35V, 0.5V, 0.6V, 0.7V, 0.8V, 0.9V and 1V. The threshold voltage of the PMOS (NMOS) transistor is 0.365V (0.325V) therefore, 0.35V is chosen as the supply voltage value for the sub-threshold INV. We simulated INVs of sizes $2\times$, $4\times$ and $15\times$. The width of the NMOS (PMOS) transistor in $2\times$ INV is $0.13\mu m$ ($0.52\mu m$). The INVs were loaded with a load capacitance of value $3\times$ of their input capacitance. The radiation particle LET values used are 2, 10 and 20 MeV-cm^2/mg, which represent low, medium and high energy strikes respectively. We also simulated a $4\times$ INV with LET = 2 MeV-cm^2/mg, and 10 MeV-cm^2/mg, and VDD = 1V for different load capacitances (0fF, 1fF, 3fF, 5fF and 6.3fF) to analyze the effect loading on the radiation susceptibility of the INV.

For each of these simulations, we assume that a radiation particle strike occurs at the center of the drain diffusion of the 3D NMOS transistor in the vertical direction (normal to the surface of the drain diffusion). Hence, in our 3D simulations we do not simulate the charge collection due to the ALPEN mechanism. The total charge collected at the drain node of the INV is due to the drift-diffusion mechanism and the bipolar effect. Physical models used in the simulations included Shockley-Reed-Hall and Auger recombination, hydrodynamic transport models for electron, bandgap narrowing dependent intrinsic carrier concentration model, mobility models which included Philips unified mobility model, high-field saturation and transverse field dependence. The silicon region containing the 3D NMOS device is about $10\mu m$ x $10\mu m$.

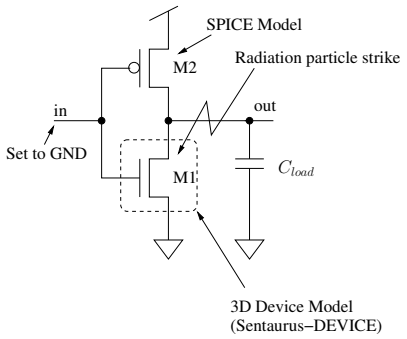

Fig. 1. Inverter (INV) under consideration

A. NMOS Device Modeling and Characterization

We constructed the 3D NMOS transistor of INV of Figure 1 using the Sentaurus-Structure editor tool [16]. The NMOS device was implemented in a 65nm bulk technology. The 3D 65nm technology model was developed based on the data available in the literature [5], [30], [31], [32], [33], [34], [28]. Based on these references, we used the gate length L = 35nm, the oxide thickness $T_{ox} = 1.2nm$, the spacer width equals to 30nm and the height of the polysilicon gate is $0.12\mu m$. We also used threshold voltage, punch through, halo and latchup implants in the NMOS device. The details of these implants are as follows. For the threshold (punch through) implant, the peak doping concentration of Boron atoms is $8e^{18}$ cm^{-3} ($7e^{18}$ cm^{-3}) at 2 nm (14 nm) below the SiO_2-channel interface, the doping concentration decreases with a Gaussian profile, and the doping concentration reduces to $1e^{17}$ cm^{-3} ($2e^{17}$ cm^{-3}) at a depth of 14 nm (5 nm) below the peak concentration surface. The peak concentration of Boron atoms for halo implants is $2e^{19}$ cm^{-3}, and these implants are in the channel region at the source-bulk and drain-bulk junctions. Again, the doping concentration reduces with a Gaussian profile. For the latchup implant, the peak doping concentration of Boron atoms is $5e^{18}$ cm^{-3} at 1.25 μm below the SiO_2-channel interface, the doping concentration decreases with a Gaussian profile, and the doping concentration reduces to $1e^{16}$ cm^{-3} at a depth of 0.4 μm. The contact of the p-well was placed at $0.75\mu m$ from the source diffusion of the NMOS transistor. We characterized the 3-D NMOS device we constructed using Sentaurus-DEVICE [16] to obtain the drain current (I_D) as a function of the drain to source voltage (VDS) for different gate to source voltages (VGS). From the $I-V$ characteristic of the NMOS transistor (not shown due to the lack of space) we observed that the NMOS device we constructed has good MOSFET characteristics. These characteristics were verified to substantially match the 65nm PTM NMOS device characteristics using SPICE.

IV. Experimental Results

Figure 2 shows the voltage at the output of the 4× INV of Figure 1 with VDD = 1V, during a radiation particle strike (of three different LET values) at the NMOS transistor. Figure 3 plots the radiation induced current through the drain terminal of the NMOS transistor of the 4× INV. Note that for a 65nm technology, as shown in Figure 2, a radiation particle with an LET value as low as 2 MeV-cm^2/mg is capable of generating a significant voltage glitch ($> 0.5VDD$). For larger LET values, the voltage at the output of the INV can become negative as shown in Figure 2 (for LET = 10 and 20MeV-cm^2/mg). Hence, 65nm devices are very susceptible to radiation particle strikes even with medium energy particles. From the plots of radiation induced NMOS drain current (shown in Figure 3), we notice that for low LET values (i.e. 2 MeV-cm^2/mg) the drain current looks like a double exponential current pulse. However, for larger LET values (i.e 10 and 20 MeV-cm^2/mg), there is plateau in the radiation induced current. As mentioned in Section II, a heavily doped substrate demonstrates charge collection due to both the drift and the diffusion processes. In deep submicron technologies such as 65nm, the substrate is heavily doped and hence, the funnel collapses very rapidly (within 10-20ps of the time of the radiation particle strike). As a result, a lot of charge is left in the substrate (after the funnel collapses) which then gets collected at the drain node of the NMOS transistor through the diffusion process [26]. This results in a significant drain current and hence, the radiation induced current remain constant for long time. Note that this process is slow, as indicated in [26]. The current plateau was not observed for LET = 2 MeV-cm^2/mg since the radiation particle deposited a small amount of charge (20 fC/μm) in the substrate and most of this charge gets collected during the funnel assisted drift collection phase. After this process, very little charge remains in the substrate, which does not result in a significant drain current.

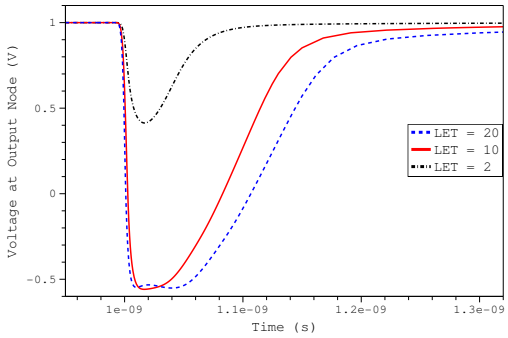

Fig. 2. Radiation induced voltage transient at the output of 4× INV with VDD=1V

The charge collected at the output of INV as a function of the supply voltage during a radiation particle strike is plotted in Figure 4, for different INV sizes and for different linear energy transfer (LETs) values. Figure 5 plots the area of the radiation induced voltage glitch (at the output of INV) for these simulations. Note that in these simulations, the INVs were loaded with a load capacitance of value 3× their input capacitance. The charge collected at the output

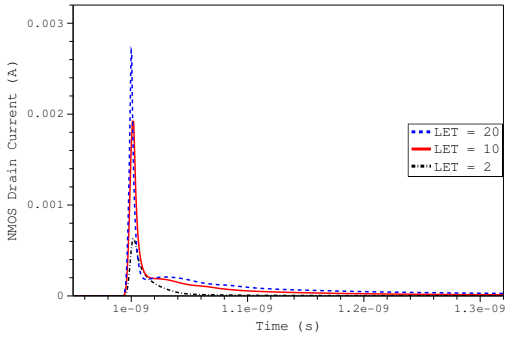

Fig. 3. Radiation induced drain current of the NMOS transistor of 4× INV with VDD=1V

of the INV is obtained by integrating the drain current of the NMOS transistor following a particle strike. The area of a voltage glitch is computed by integrating the difference of the supply voltage and the voltage at the output of INV ($VDD - V(out)$) following a radiation particle strike. Thus, for a radiation particle strike at time $t1$ at the drain of M1 of the INV shown in Figure 1, the charge collected at out is $Q_{coll} = \int_{t=t1}^{\infty} I_d^{M1} dt$ and the area of the voltage glitch is $\int_{t=t1}^{\infty} (VDD - V(out))dt$. Note that the area of the radiation induced voltage glitch is a good measure of the susceptibility of an INV (or any gate) to radiation particle strikes, because it incorporates both the magnitude as well as the duration of the voltage glitch. It also allows us to compare the susceptibility of INVs across different supply voltage values. From Figures 4 and 5 we make several observations. These observations, along with their explanation are as follows.

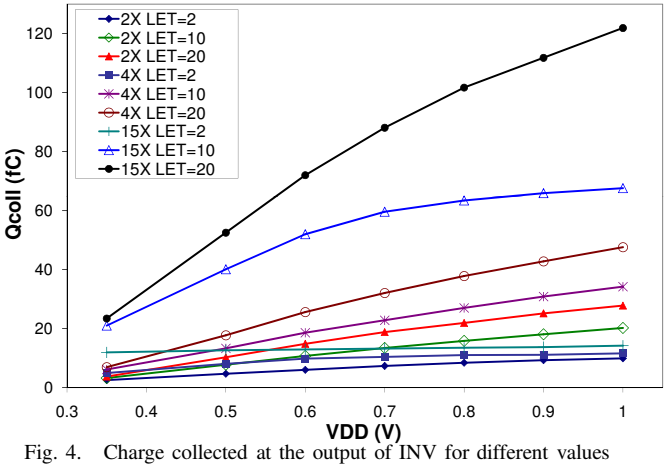

Fig. 4. Charge collected at the output of INV for different values

1) The effects of radiation particle strikes become severe for supply voltages less than 60% of the nominal value (which is slightly lower than the twice of the threshold voltage of the PMOS transistor). As shown in Figure 5, the area of the voltage glitch increases with decreasing supply voltages. The PMOS transistor of the INV is primarily responsible for recovering the voltage at the output node during a radiation particle strike at the NMOS transistor. As the supply voltage (VDD) is decreased, the PMOS transistor drive strength reduces and the PMOS transistor becomes significantly weaker when the supply voltage is reduced below $2 \cdot V_T^P$. Note

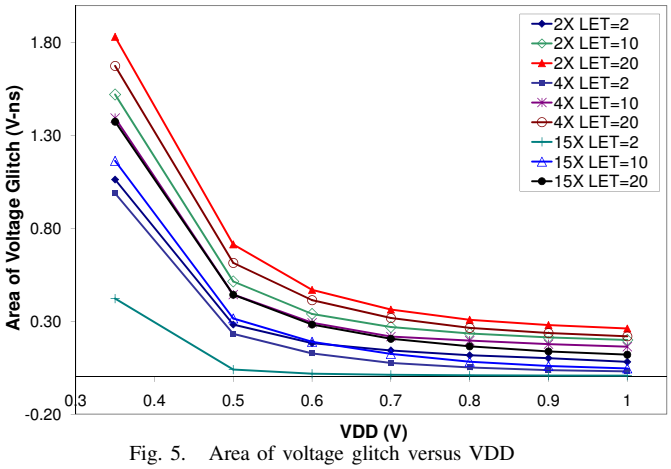

Fig. 5. Area of voltage glitch versus VDD

that the decrease in the drive strength of the PMOS transistor with decreasing VDD value is much higher for VDD $< 2 \cdot V_T^P$ compared to VDD values greater $2 \cdot V_T^P$. Hence, when the supply voltage is less than $2 \cdot V_T^P$ than the PMOS transistor takes longer to recover the voltage at the output of the INV.

2) The amount of charge collected due to a radiation particle strike reduces with decreasing supply voltage. The charge collected due to the funnel-assisted drift process depends on the strength of the electric field in the drain-bulk junction. At lower voltages, the electric field in the drain-bulk junction is weaker than at higher voltages. Also, the drain voltage of the device takes longer to fall for higher supply voltages compared to lower supply voltages. Therefore, in case of high supply voltages, the electric field in the drain-bulk junction is strong and present for a longer duration of time, due to which a large amount of charge gets collected at the drain node (compared to the case when the supply voltage is low).

Along with the two observations mentioned above, we also noted the following phenomenons.

1) Small devices collect less of the charge deposited by a radiation particle, compared to larger devices. This phenomenon occurs mainly due to two reasons i) in a small device, the drain node falls more quickly compared to a large device. Therefore, the strong electric field in the drain-bulk junction of the NMOS exists for shorter duration of time in the small device than in the large device. Thus, less charge is collected initially during the funnel assisted drift collection phase for a small device. ii) the drain area is smaller in a small device compared to a large device. As a result, less charge is collected through the diffusion process in the small device.
2) For low energy radiation particle strikes, wide devices collect almost the same amount of charge across different supply voltage values. In other words, the charge collection efficiency of wide devices is high and largely independent of supply voltage. As mentioned earlier, during a low energy radiation particle most of the deposited charge gets collected within a few picoseconds after the particle strike. Also, in a wide device, the drain of the device takes longer to fall, even for low supply voltages, during a low energy radiation strike. Thus, the electric field is present in the drain-bulk junction for a long duration of time and a significant amount of charge get collected, even at low supply voltages.

To analyze the effect of loading on the radiation susceptibility of a gate, we also simulated a 4× INV with LET = 2 MeV-cm^2/mg and 10 MeV-cm^2/mg, and VDD = 1V for different load capacitances (0 fF, 1fF, 3fF, 5fF and 6.3fF). The results are reported in Table I. In Table I, Columns 1 and 2 report the LET and the load capacitance values under consideration. Column 3 reports the charge collected (Q_{coll}) at the output of the INV. The area of the radiation induced voltage glitch is reported in Column 4. From Table I we make the following observations:

1) For small devices with medium or high energy radiation particle strikes, the pulse width of the voltage glitch *increases* with an increasing load capacitance (C_{load}) of the gate. Due to a radiation particle strike of medium (or high) energy, the voltage at the output of the INV of smaller sizes (such as 4× or smaller) becomes negative very rapidly. After this the PMOS transistor of the INV starts recovering the voltage at the output. If the INV is driving a higher load capacitance (C_{load}), then the PMOS will take longer time to restore the output voltage. Thus, the width of the voltage glitch increases or radiation tolerance of the INV reduces with the increasing load capacitance (C_{load}), contrary to popular belief (which says that increasing load capacitance improves the radiation tolerance of gates).
2) However, for low energy radiation particle strikes, an increasing load capacitance (C_{load}) of the gate *improves* the radiation tolerance of the INV. The magnitude of the voltage glitch is reduced with the increasing load capacitance (which is due to increasing fanout). This effect is more visible for low energy radiation particle strikes. For high energy strikes, the difference in the magnitude of the voltage glitch for two different loads is very small. As the voltage glitch magnitude is lower for low energy strikes, the PMOS transistor of the INV has to recover a lower voltage swing at the output node. Thus, the width of the voltage glitch reduces with the increasing fanout load. Hence, the INV becomes more tolerant to low energy radiation strikes with the increasing load capacitance.
3) The charge collected increases with the increasing load capacitance. This is again due to fact that the voltage of the drain node of the NMOS transistor falls slowly for large load capacitances. Thus, the electric field is present in the drain-bulk junction of the NMOS for a longer duration and hence, more charge gets collected.

The observations made above from Figure 4 and 5, and Table I are important to consider during radiation hardening

LET	C_{load} (fF)	Q_{coll} (fC)	Voltage Glitch
(MeV-cm^2/mg)			Area (V-ns)
2	0	10.0	0.0434
2	1	10.9	0.0448
2	3	11.1	0.0361
2	5	11.3	0.0314
2	6.3	11.6	0.0303
10	0	26.8	0.1224
10	1	27.7	0.1284
10	3	29.9	0.1409
10	5	32.6	0.1549
10	6.3	34.2	0.1629

TABLE I

Q_{coll} AND AREA OF VOLTAGE GLITCH VERSUS LOAD CAPACITANCE (C_{load})

of DVS and sub-threshold circuits. Based on the observations made, we present some design guidelines for DVS and sub-threshold circuits. These guidelines suggest that the traditional radiation hardening approaches need to be modified or revisited for DVS and sub-threshold circuits.

1) DVS designs should scale down the supply voltage of a circuit to $2 \cdot V_T$ (V_T is the maximum of V_T^P and V_T^N). Below this value, radiation susceptibility increases rapidly as shown in Figure 5. Also, a circuit with DVS should be hardened at the *lowest* operating voltage, with the charge collected at that voltage. This will ensure radiation tolerance at higher supply voltages. Sub-threshold circuits and circuits with a supply voltage $< 2 \cdot V_T$ require aggressive protection against radiation strikes.
2) If a gate is upsized to increase its radiation tolerance (as proposed in [18]), then a higher value of charge collected due to a radiation particle strike should be used. This is extremely important for low voltage operation, since lowered voltage circuits are more likely to have large voltage glitch areas.
3) For environments with low energy radiation particles, it is safe to assume that the charge collected remains constant across different supply voltages for wide devices. The collected charge also remains roughly constant across different gate sizes for high or nominal voltage operation.
4) The fanout load capacitance (C_{load}) of gates should be kept low in circuits operating in high energy radiation particle environments. This is contrary to conventional wisdom. For low energy radiation environments, the fanout factor (load capacitance) of the gates should be increased to improve their radiation tolerance.

A. Charge Collection Model for DVS Circuits

From Figure 4 we observe that the charge collected (Q_{coll}) at the output of a gate has a strong dependence on the size of the gate, the supply voltage (VDD) and the radiation particle energy (LET). Therefore, simulating radiation particle strikes in DVS circuits in SPICE using a worst case collected charge (maximum possible charge collection) may lead to very pessimistic designs. To improve the accuracy of SPICE simulations of radiation particle strikes in DVS circuits, we propose a model for the charge collected (Q_{coll}^M) at the output node of gate, and append 4 parameters from this model in to the SPICE model cards for MOSFETs (for example, the PTM model cards for 65nm [29]). Since Q_{coll} directly depends on the size of a gate - W (expressed in μm), VDD and LET (expressed in MeV-cm^2/mg), we propose that $Q_{coll}^M = min(K_{MAX} \cdot LET, K_Q \cdot W^{\beta_1} VDD^{\beta_2} LET^{\beta_3})$. Here, K_{MAX}, K_Q, β_1, β_2 and β_3 are obtained by characterizing a process technology through 3D simulations of radiation particle strikes. In the expression for Q_{coll}^M, $K_{MAX} \cdot LET$ represents the maximum amount of charge that can be collected due to a radiation particle strike. The value of K_{MAX} is obtained from 3D simulations of radiation particle strikes at the drain of a very wide NMOS transistor for different LET values. Note that the drain terminal of this NMOS transistor was connected to VDD (nominal value) and the source, gate and bulk terminals were connected to GND to maximize the charge collection. From 3D simulations, K_{MAX} was found to be 0.8. We obtained the values of K_Q, β_1, β_2 and β_3 by fitting the model Q_{coll}^M with Q_{coll} obtained through 3D simulations (shown in Figure 4) for 2×, 4× and 15× INV for VDD = 0.6 to 1.0 V (in steps of 0.1V) and LET = 10 and 20 MeV-cm^2/mg. The values we obtained are $K_Q = 16.54$, $\beta_1 = 0.704$, $\beta_2 = 0.9$ and $\beta_3 = 0.664$. Note that we performed the curve fit for medium and high energy particles, since hardening of DVS circuits need to be performed against radiation particles of such energies to meaningfully improve their radiation tolerance. As mentioned earlier, for low energy particle strikes, it is safe to assume that the charge collected remains constant across different supply voltages in wide transistors. Therefore, our model Q_{coll}^M is applicable for medium and high energy particle strikes. Also, as we have proposed, DVS designs should scale the supply voltages of a circuit up to 60% of the nominal value, and therefore the model Q_{coll}^M is obtained for VDD = 0.6 to 1.0 V. To evaluate the accuracy of our model, we plotted the charge collected at the output of the INV (shown in Figure 1) predicted by our model (dark bar) and from 3D simulations (light bar) in Figure 6. Figure 6 shows the charge collected with VDD = 0.6 to 1.0 V in steps of 0.1 V as the outermost variable. For each voltage value the charge collected is reported for 2×, 4× and 15× INVs with LET = 10 and 20 MeV-cm^2/mg, as the legend indicates. We observe from Figure 6 that our model is very accurate, with an average error of 6.3%. Thus, our model can improve the accuracy of the SPICE level simulation of radiation particle strikes in DVS circuits. For sub-threshold circuits, it is difficult to find an accurate model since the charge collection efficiency is very low and hence, 3D simulations have to be used to obtain the value of the charge collected (Q_{coll}) at the output node of a gate for different parameter values (W and LET).

V. CONCLUSIONS

Single event upsets (SEUs) are becoming increasingly important problems for both combinational and sequential circuits. At the same time, power has become a major issue in computing. In recent times, it is common to decrease

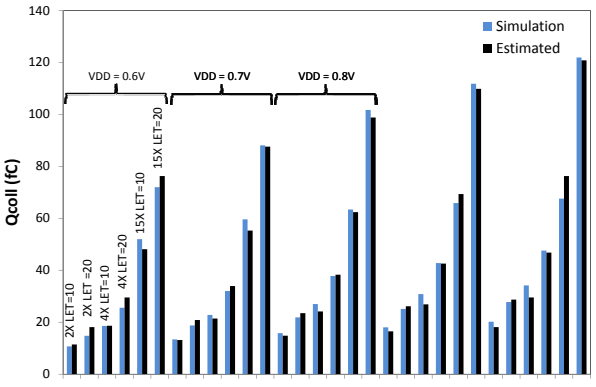

Fig. 6. Comparison of charge collected (Q_{coll}) obtained from our model versus 3D simulations

the supply voltage value in the non-critical parts of VLSI systems, in order to reduce the power and energy consumption. Reduced supply voltages further aggravate the reliability issue due to SEUs. With increasing demand for reliable systems, it is necessary to design radiation tolerant circuits efficiently. In this paper, we have analyzed radiation particle strikes in DVS and sub-threshold circuits. We performed 3D simulations for radiation particle strikes in an inverter, using Sentaurus-DEVICE. We analyzed the sensitivity of DVS and sub-threshold circuits to radiation particle strikes by varying the inverter size, the inverter load, the supply voltage (VDD) and the energy of the radiation particle in our simulations. From these 3D simulations, we make several observations which are important to consider during radiation hardening of DVS and sub-threshold circuits. Based on these observations, we propose several guidelines for radiation hardening of DVS and sub-threshold circuit designs. We also proposed an accurate model for the charge collected in DVS circuits.

REFERENCES

[1] T. May and M. Woods, "Alpha-particle-induced soft errors in dynamic memories," *IEEE Trans. on Electron Devices*, vol. ED-26, pp. 2–9, jan 1979.

[2] J. Pickle and J. Blandford, "CMOS RAM cosmic-ray-induced error rate analysis," *IEEE Trans. on Nuclear Science*, vol. NS-29, pp. 3962–3967, 1981.

[3] P. Shivakumar, M. Kistler, S. W. Keckler, D. Burger, and L. Alvisi, "Modeling the effect of technology trends on the soft error rate of combinational logic," in *DSN '02: Proceedings of the 2002 International Conference on Dependable Systems and Networks*, 2002, pp. 389–398.

[4] P. Dodd and L. Massengill, "Basic mechanisms and modeling of single-event upset in digital microelectronics," *IEEE Transactions on Nuclear Science*, vol. 50, no. 3, pp. 583– 602, 2003.

[5] "The International Technology Roadmap for Semiconductors," `http://public.itrs.net/`, 2003.

[6] W. Kim, D. Shin, H. Yun, J. Kim, and S. Min, "Performance comparison of dynamic voltage scaling algorithms for hard real-time systems," in *Proc. of IEEE Real-Time and Embedded Technology and Applications Symposium*, 2002, pp. 219–228.

[7] B. Zhai, D. Blaauw, D. Sylvester, and K. Flautner, "Theoretical and practical limits of dynamic voltage scaling," in *DAC*, 2004, pp. 868–873.

[8] C. Duan and S. P. Khatri, "Computing during supply voltage switching in DVS enabled real-time processors," in *Proc. of the Intl. Symposium on Circuits and Systems*, May 2006.

[9] S.-H. Choi, B.-K. Kim, J. Park, C.-H. Kang, and D.-S. Eom, "An implementation of wireless sensor network," *IEEE Transactions on Consumer Electronics*, vol. 50, no. 1, pp. 236–244, Feb 2004.

[10] A. Abidi, G. Pottie, and W. Kaiser, "Power-conscious design of wireless circuits and systems," *Proceedings of the IEEE*, vol. 88, no. 10, pp. 1528–1545, Oct 2000.

[11] N. Jayakumar, R. Garg, B. Gamache, and S. P. Khatri, "A PLA based asynchronous micropipelining approach for subthreshold circuit design," in *DAC '06: Proceedings of the 43rd annual conference on Design automation*. New York, NY, USA: ACM Press, 2006, pp. 419–424.

[12] J.-M. Palau, M.-C. Calvet, P. Dodd, F. Sexton, and P. Roche, "Contribution of device simulation to SER understandfng," *Reliability Physics Symposium Proceedings, 2003. 41st Annual. 2003 IEEE International*, pp. 71–75, March 2003.

[13] F. Irom, F. Farmanesh, A. Johnston, G. Swift, and D. Millward, "Single-event upset in commercial silicon-on-insulator PowerPC microprocessors," *Nuclear Science, IEEE Transactions on*, vol. 49, no. 6, pp. 3148–3155, Dec 2002.

[14] O. Flament, J. Baggio, C. D'hose, G. Gasiot, and J. Leray, "14 MeV neutron-induced SEU in SRAM devices," *Nuclear Science, IEEE Transactions on*, vol. 51, no. 5, pp. 2908–2911, Oct. 2004.

[15] P. Hazucha, C. Svensson, and S. Wender, "Cosmic-ray soft error rate characterization of a standard 0.6-μm CMOS process," *Solid-State Circuits, IEEE Journal of*, vol. 35, no. 10, pp. 1422–1429, Oct 2000.

[16] Synopsys Inc., "Sentaurus user's manual, vol. 2007.12."

[17] A. Ejlali, B. M. Al-Hashimi, M. T. Schmitz, P. Rosinger, and S. G. Miremadi, "Combined time and information redundancy for SEU-tolerance in energy-efficient real-time systems," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 14, no. 4, 2006.

[18] Q. Zhou and K. Mohanram, "Gate sizing to radiation harden combinational logic," in *Proceedings, Computer-Aided Design of Integrated Circuits and Systems*, Jan 2006, pp. 155–166.

[19] K. Mohanram and N. A. Touba, "Cost-effective approach for reducing soft error failure rate in logic circuits," in *ITC*, 2003, pp. 893–901.

[20] R. Garg, N. Jayakumar, S. P. Khatri, and G. Choi, "A design approach for radiation-hard digital electronics," in *Proceedings, IEEE/ACM Design Automation Conference (DAC)*, July 2006, pp. 773–778.

[21] L. Edmonds, "A simple estimate of funneling-assisted charge collection," *Nuclear Science, IEEE Transactions on*, vol. 38, no. 2, pp. 828–833, Apr 1991.

[22] P. Dodd, F. Sexton, and P. Winokur, "Three-dimensional simulation of charge collection and multiple-bit upset in Si devices," *IEEE Trans. Nuclear Science*, vol. 41, pp. 2005–2017, 1994.

[23] P. Dodd, "Device simulation of charge collection and single-event upset," *Nuclear Science, IEEE Transactions on*, vol. 43, no. 2, pp. 561–575, Apr 1996.

[24] P. Dodd, F. Sexton, G. Hash, M. Shaneyfelt, B. Draper, A. Farino, and R. Flores, "Impact of technology trends on SEU in CMOS SRAMs," *Nuclear Science, IEEE Transactions on*, vol. 43, no. 6, pp. 2797–2804, Dec 1996.

[25] A. Johnston, "Scaling and technology issues for soft error rate," in *Proc. Annual Research Conference on Reliability*, oct 2000.

[26] R. Baumann, "Soft errors in advanced computer systems," *Design & Test of Computers, IEEE*, vol. 22, no. 3, pp. 258–266, May-June 2005.

[27] G. Messenger, "Collection of charge on junction nodes from ion tracks," *IEEE Trans. Nuclear Science*, vol. 29, no. 6, pp. 2024–2031, 1982.

[28] S. DasGupta, "Treands in single event pulse widths and pulse shapes in deep submicron CMOS," Master's thesis, Vanderbilt University, 2008.

[29] PTM, http://www.eas.asu.edu/ ptm.

[30] P. Bai et al., "A 65nm logic technology featuring 35nm gate lengths, enhanced channel strain, 8 Cu interconnect layers, low-k ILD and 0.57μm^2 SRAM cell," *Electron Devices Meeting, 2004. IEDM Technical Digest. IEEE International*, pp. 657–660, Dec. 2004.

[31] S.-Y. Chen, H.-S. Huang, H.-C. Lin, L.-C. Shie, and M.-Q. Chen, "Using simulation for characterize high performance 65nm node planar N-MOSFETs," in *2004 International Symposium on NANO Science and Technology*, Nov 2004.

[32] Y. Taur and E. J. Nowak, "CMOS devices below 0.1 um: How high will performance go?" *Electron Devices Meeting, 2004. IEDM Technical Digest. IEEE International*, pp. 215–218, Dec. 1997.

[33] T. Fukai et al., "A 65 nm-node CMOS technology with highly reliable triple gate oxide suitable for power-considered system-on-a-chip," *VLSI Technology, 2003. Digest of Technical Papers. 2003 Symposium on*, pp. 83–84, June 2003.

[34] O. A. Amusan, "Analysis of single event vulnerabilities in a 130 nm CMOS technology," Master's thesis, Vanderbilt University, 2006.